THREAD-AWARE INSTRUCTION FETCHING IN A MULTITHREADED EMBEDDED PROCESSOR

ABSTRACT OF THE DISCLOSURE

[0079] The present invention provides a multithreaded processor, such as a network processor, that fetches instructions in a pipeline stage based on feedback signals from later stages. The multithreaded processor comprises a pipeline with an instruction unit in the early stage and an instruction queue, a thread interleaver, and an execution pipeline in the later stages. Feedback signals from the later stages cause the instruction unit to block fetching, immediately fetch, raise priority, or lower priority for a particular thread. The instruction queue generates a queue signal, on a per thread basis, responsive to a thread queue condition, etc., the thread interleaver generates an interleaver signal responsive to a thread condition, etc., and the execution pipeline generates an execution signal responsive to an execution stall, etc.